

Appl. No. 10/581,880
Request for Corrected Filing Receipt dated 03/19/2007
Attorney Docket No. 1217-052989

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/581,880 Confirmation No. 1955
Applicants : Tatsuo KATAOKA et al.
Filed : June 5, 2006
Title : Printed Wiring Board, Its Manufacturing Method, and Circuit Device
Art Unit : 2812
Examiner :
Customer No. : 28289

FACSIMILE NO. 703-305-9822
Office of Initial Patent Examination's
Filing Receipt Corrections
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P.O. Box 1450
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REQUEST FOR CORRECTED FILING RECEIPT

Sir:

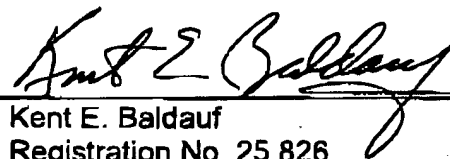
Attached is a marked-up copy of the official Filing Receipt for the above-identified patent application for which a Corrected Filing Receipt is hereby requested. The priority date is incorrect and should read as follows: -- 12/02/2004 --

Copies of the WO front page and page 1 of the Declaration and Power of Attorney are enclosed for verification.

Respectfully submitted,

THE WEBB LAW FIRM

By



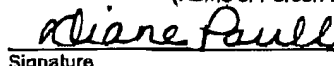
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FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date set forth below.

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Signature

3/19/2007

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
10/581,880	06/05/2006	2812	900	1217-052989	4	14	2

CONFIRMATION NO. 1955

FILING RECEIPT

28289

THE WEBB LAW FIRM, P.C.
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Date Mailed: 03/02/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

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Assignment For Published Patent Application

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Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP04/17945 09/02/2004

-- 12/02/2004

Foreign Applications

JAPAN 2003-407540 12/05/2003

JAPAN 2004-222184 07/29/2004

If Required, Foreign Filing License Granted: 02/08/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is
US10/581,880

Projected Publication Date: 05/17/2007

Non-Publication Request: No

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Declaration and Power of Attorney for Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PRINTED WIRING BOARD, MANUFACTURING PROCESS AND CIRCUIT DEVICE

The specification of which

- ☐ is attached hereto.
- ☐ was filed on _____
as Application Serial No. _____
and was amended on _____
(if applicable)
- ☒ was filed as PCT international application
No. PCT/JP2004/17945 on December 2, 2004
and was amended under PCT Article 19 on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
<u>2003-407540</u>	<u>Japan</u>	<u>5 December 2003</u>	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No
(Number)	(Country)	(Day/Month/Year Filed)		
<u>2004-222184</u>	<u>Japan</u>	<u>29 July 2004</u>	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No
(Number)	(Country)	(Day/Month/Year Filed)		
_____	_____	_____	<input type="checkbox"/> Yes	<input type="checkbox"/> No
(Number)	(Country)	(Day/Month/Year Filed)		

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(19) 世界知的所有權機關
國際事務局



(43) 國際公開日
2005 年 6 月 16 日 (16.06.2005)

PCT

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(51) 國際特許分類: H05K 3/06

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(21) 国际出版号: PCT/JP2004/017945

(72) 発明者: および

(22) 國際出版日: (2004 年 12 月 3 日)(02.12.2004)

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(25) 國際出願の言語: 日本語

(26) 國際公開の言語: 日本語

(30) 優先権データ:

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特願2004-222184	2004年7月29日(29.07.2004)	JP

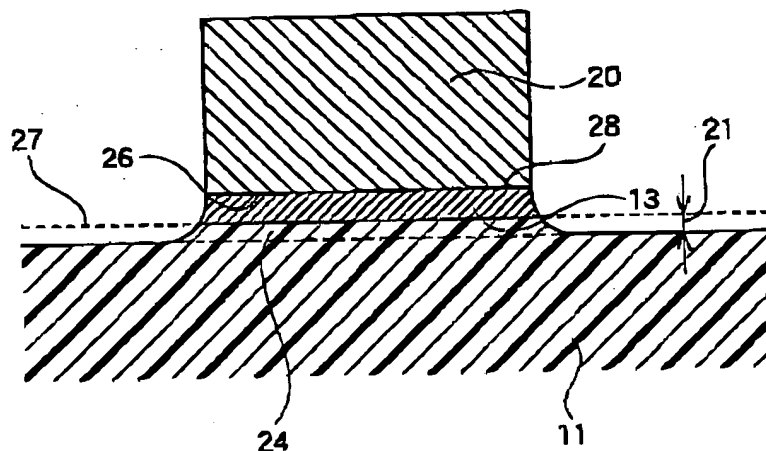
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〔統葉有〕

(S4) Title: PRINTED WIRING BOARD, ITS MANUFACTURING METHOD, AND CIRCUIT DEVICE

(54) 発明の名称: プリント配線基板、その製造法および回路装置



(57) Abstract: [MEANS FOR SOLVING PROBLEMS] A method of manufacturing a printed wiring board is characterized in that a conductive metal layer is formed over at least one surface of an insulating film via a sputtering metal layer. the sputtering metal layer and the conductive metal layer are removed selectively by etching so as to form a wiring pattern, the multilayer film is treated with a first treating liquid capable of dissolving Ni contained in the sputtering metal layer and treated with a second treating liquid capable of dissolving Cr contained in the sputtering metal layer and removing the sputtering metal layer on the insulating film, and the sputtering metal remaining on the portion of the surface layer of the insulating film on which the wiring pattern is not formed is removed together with the insulating film surface layer. A printed wiring board is characterized in that the thickness of the portion of the insulating film on which the wiring pattern is not formed is smaller by 1 to 100 nm than that of the portion of the insulating film on which the wiring pattern is formed. The sputtering metal bonded to the insulating film is removed together with the insulating film and no metal remains on the surface of the portion of the insulating film between the wiring patterns. Therefore, a short circuit between the wiring patterns hardly occurs.

(57) 要約: 【解決手段】 本発明のプリント配線基板の製造法は、絶縁フィルムの少なくとも一方の表面に、スパッタリング金属層を介して積層された導電性金属を形成し、該スパッタリング金属層および導電性金属層を、エッチング法により選択的に除去して配線パターンを形成した後、該積層フィルムを、ス

「統策有」

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